UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,092	05/23/2001	Mark Thomas McCormack	078523.0102	5484

5073 7590 11/26/2007

BAKER BOTTS L.L.P.
2001 ROSS AVENUE
SUITE 600
DALLAS, TX 75201-2980

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
11/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptomail1@bakerbotts.com
glenda.orrantia@bakerbotts.com

TH

Office Action Summary	Application No.	Applicant(s)	
	09/866,092	MCCORMACK ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-24,26-34 and 36-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-24,26-34 and 36-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

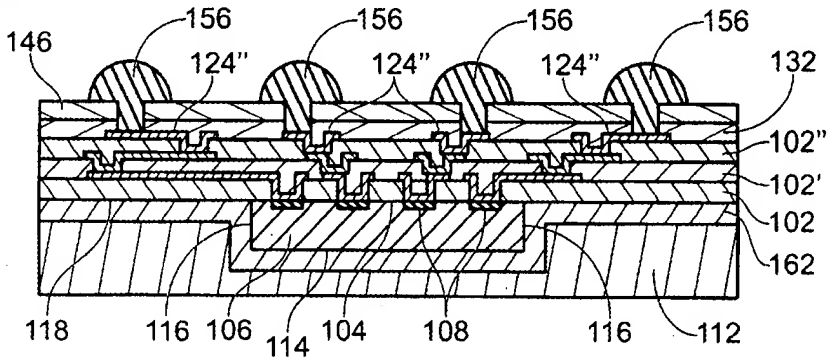
Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 33, 34, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. 6,154,366 in view of Wojnarowski et al. 5,866,952 in view of Higashi et al. 6,861,284 B2. Ma discloses (see, for example, Fig. 2j) a package (multi-layer printed circuit board) comprising an encapsulation material (circuit board substrate) 112 having a first substrate surface and a second substrate surface, die (first integrated electronic component) 106, cavity, flex component (first dielectric layer) 102, conductive trace (metallic layer) 124, electrically conductive first via, element (second dielectric layer) 102', and electrically conductive second via.

Fig. 2j



Ma does not disclose the circuit board substrate being polymeric. However, Wojnarowski discloses (see, for example, FIG. 1(e)) an integrated module substrate comprising a chip 14, and substrate molding material (circuit board substrate) 24. In column 7, lines 50-62, Wojnarowski discloses the substrate molding material being polymers (polymeric). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die in a substrate form, and any overlying layers wherein the material is not prone to cracking.

Ma in view of Wojnarowski does not disclose a second electrically conductive via extending at one location. However, Higashi discloses (see, for example, Fig. 7) a substrate 10 comprising a wiring pattern (second electrically conductive via) 18 in a via hole. The wiring traverses multiple insulating layers. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second electrically conductive via extending at one location in order to lessen manufacture time, and save material.

Regarding claims 33, and 34, Ma discloses (see, for example, FIG. 1d) multiple conductive traces (at least one metal-lined via) 124. The multiple conductive traces transmit signals to the die.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Wojnarowski in view of Higashi.

3. Claims 18, 20 thru 23, 27, 30, 36, 40, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 and further in view of Miura et al. 5,565,706. Ma in view of Wojnarowski in view of Higashi does not disclose a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface. Miura discloses (see, for example, FIG. 6) a multi-layer package board (multi-layer printed circuit board) comprising a package board 46 having external output terminals (first metallic layer) 8 and external output terminals (second metallic layer) 28. It would have been obvious to one of ordinary skill in the art at the time of invention to have a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface in order to include external connections to the substrate such as voltages, metallizations, etc.

Regarding claims 20-23, see, for example, FIG. 6 wherein Miura discloses a via going through the package board 46 that connects the exteran louput terminals and other metal layers in the dielectric layers.

Regarding claim 27, see figures wherein Miura discloses external output terminals (conductive pad) 8 on top of the LSI 35.

Regarding claim 30, see FIG. 6 wherein Miura discloses one of the vias (at least one metal-lined via) 16 attached to LSI 33.

Regarding claim 36, see, for example, column 8, lines 25-28 wherein Miura discloses a capacitor.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 above, and further in view of Desai 5,739,188. Ma in view of Wojnarowski in view of Higashi does not disclose the multi-layer core substrate comprising at least two polymeric layers. However, Desai discloses (see, for example, column 3, lines 26-30) a multi layered product wherein the product comprises a substrate layer/cap layer (two polymeric layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the multi-layer core substrate comprising at least two polymeric layers in order to protect the substrate.

5. Claims 24, 26, 28, 29, 31, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Marcinkiewicz et al. 5,241,456. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity. However, Marcinkiewicz discloses (see, for example, FIG. 1) a structure 10 comprising a substrate 12, and chip (second integrated electronic component) 36. Having the chip in the same substrate creates a multichip device that saves space and provides interconnection between two chips. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component

disposed in said cavity in order to create a multichip device that saves space and provides interconnection between two chips.

Regarding claim 28, see, for example, FIG. 1 wherein Marcinkiewicz discloses contact pad (conductive pad) 38.

Regarding claim 29, see, for example, FIG. 1 wherein Miura discloses contact pad (conductive pad) 8 on top of the LSI 35.

Regarding claim 44, Miura in view of Wojnarowski in view of Higashi in view of Miura does not disclose a third dielectric layer disposed on said second side of said substrate. However, Marcinkiewicz discloses (see, for example, FIG. 1) a substrate 12, and dielectric layer (third dielectric layer) 52. The dielectric layer protects the bottom surface of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a third dielectric layer disposed on said second side of said substrate in order to protect the bottom of the substrate.

6. Claims 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Miyazawa et al. 5,953,619. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said capacitor comprising a perovskite capacitance material. However, Miyazawa discloses (see, for example, column 1, lines 27-35) that a perovskite crystal structure has a high dielectric constant. Therefore, it would have been obvious to one of ordinary skill in

the art at the time of invention to have said capacitor comprising a perovskite capacitance material in order to have a higher dielectric constant in the same area.

Response to Arguments

7. Applicant's arguments filed 9/6/07 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 9 of the response filed 9/6/07 that Ma does not disclose a substrate having a cavity formed in a substrate, this argument is not persuasive. In Fig. 2j, Ma clearly discloses a circuit board substrate having a cavity wherein the cavity contains a first integrated electronic component 106. There is a moisture barrier layer 162, however, this moisture barrier layer does not preclude the fact that the first integrated electronic component is attached in the cavity (by way of the moisture barrier layer). The applicant's argument regarding technique is not persuasive because the claims are directed towards product, not process, and the claimed **structural** limitations are clearly disclosed by Ma in view of Wojnarowski in view of Higashi regardless of whether the multi-layer printed circuit board was made using the same method. Please see ***Product-by-Process Limitations*** paragraph below.

Product-by-Process Limitations

While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re*

Wethheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Regarding the applicant's argument on the bottom of page 9 that the Office Action has not provided a sufficient basis for combining the teachings of Ma with those of Wojnarowski, this argument is not persuasive. The Examiner recognizes that references can not be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is NO requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969). In this case, it would have been obvious to one of ordinary skill in the art to use polymers for the substrate in order to support a die, and any overlying layers, wherein the material is not prone to cracking. Wojnarowski shows (i.e. Fig. 1(e)) this to be true wherein Fig. 1(e) discloses a die 14 on a substrate 24 wherein the die is in a cavity. The applicant's argument on page 11

regarding Miura is also not persuasive for the same reason (i.e. there is NO requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art). Miura discloses (see, for example, FIG. 6) a die 33 in a substrate 45 wherein the die is in a cavity. Miura shows that this same die can have additional connections wherein the connections are on a polymeric substrate. Such a modification would be beneficial in order to connect dies to other dies and/or devices to make more robust devices (i.e. processors, etc).

Regarding the applicant's argument on page 12 that Desai teaches a wholly different art, this argument is not persuasive. It has been held that the determination that a reference is from a non-analogous art is two fold. First, we decide if the reference is within the field of the inventor's endeavor. If it is not, we proceed to determine whether the reference is reasonably pertinent to the particular problem with which the inventor was involved. In re Wood, 202 USPQ 171, 174. In this case, Desai teaches (see, for example, column 3, lines 28-31) how thermoplastic materials (like Ma in view of Wojnarowski in view of Higashi also teach these materials) can be divided into two separate layers wherein one layer is the core and the other layer is protective. Applicant cites the cap layer may also hide imperfections of the core which would also be applicable (and beneficial) to Ma in view of Wojnarowski in view of Higashi. Since Ma in view of Wojnarowski in view of Higashi discloses polymeric substrates, and Desai also discloses polymeric materials in general, it would have been obvious to one of ordinary skill in the art to combine Desai's teaching into Ma in view of Wojnarowski in view of Higashi in order to have the same benefits.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
November 16, 2007

EUGENE LEE
PRIMARY EXAMINER